IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

MAURICE MITCHELL INNOVATIONS, L.P.	§	
	§	
Plaintiff	§	
	§	**CASE NO. 2:04-CV-450**
vs.	§	
	§	
INTEL CORPORATION,	§	
Defendant	§	

MEMORANDUM OPINION

This Claim Construction Opinion construes terms in United States Patent No. 4,875,154 ("the '154 patent").

BACKGROUND

Plaintiff Maurice Mitchell Innovations, L.P. ("Mitchell") alleges that Defendant Intel Corporation ("Intel") infringes claim 1 of the '154 patent. In general, the '154 patent discloses what the patent refers to as a "Bimemory Independent CPU ('central processing unit')" microcomputer, also referred to as a "BICPU microcomputer." According to the specification, the BICPU microcomputer

> is comprised of a known CPU chip with additional circuitry to enable the CPU to interact in a multi BICPU microcomputer system. Each BICPU microcomputer within a system is supplied with an assigned standard memory-mechanically and logically connected to its BICPU's "A" bus circuits. The BICPU microcomputer is also provided with connectors enabling the CPU to be connected to system buses.

Col. 7:3-12. In general terms, the specification says that the invention allows a number of BICPU microcomputers to be linked together in a "bimemory independent pattern" using a "standard" set of system buses to mechanically interconnect "B" or "C" bus circuits of any two BICPU microcomputers. Col. 7:12-22.

Limitations from claim 1 of the '154 patent have been previously construed by United States District Judge Susan Illston of the United States District Court for the Northern District of California in *Maurice Mitchell v. Samsung Electronics Co., Ltd.*, No. C 01-0295 SI, (N.D. Cal. Jan. 29, 2002). The parties have agreed to adopt Judge Illston's construction for most of the terms in claim 1 of the '154 patent.

APPLICABLE LAW

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). In claim construction, courts examine the patent's intrinsic evidence to define the patented invention's scope. *See id.*; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). This intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312-13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim

does not include the limitation. *Id*. at 1314-15. Claims "must be read in view of the specification, of which they are a part." *Id*. at 1315. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 978 (Fed. Cir. 1995)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. Also, the specification may resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. But, "although the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims." *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but

technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition is entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

The patent in suit also contains means-plus-function limitations that require construction. Where a claim limitation is expressed in "means plus function" language and does not recite definite structure in support of its function, the limitation is subject to 35 U.S.C. § 112, ¶ 6. *Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). In relevant part, 35 U.S.C. § 112, ¶ 6 mandates that "such a claim limitation 'be construed to cover the corresponding structure . . . described in the specification and equivalents thereof.'" *Id*. (citing 35 U.S.C. § 112, ¶ 6). Accordingly, when faced with means-plus-function limitations, courts "must turn to the written description of the patent to find the structure that corresponds to the means recited in the [limitations]." *Id*.

Construing a means-plus-function limitation involves multiple inquiries. "The first step in construing [a means-plus-function] limitation is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). Once a court has determined the limitation's function, "the next step is to determine the corresponding structure disclosed in the specification . . . ." *Id*. A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id*. Moreover, the focus of the "corresponding structure" inquiry is not merely whether a structure is capable of

performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id*.

THE '154 PATENT[1]

"*a microcomputer data processing apparatus, comprising*"

The Court and the parties agree that the phrase should be construed as "a single microcomputer, which includes, at the least, a microprocessor, storage (*e.g.* memory) and input/output device enabling the system to perform operations on data, which comprises what is set forth in the claim."

"*a central processing unit (CPU)*"

The Court and the parties agree that the term should be construed as "the unit of a computing system having the circuits that control the interpretation of instructions and their execution. A CPU includes, at least, an arithmetic logic unit and associated registers."

"*a path configuring means*"

The central dispute between the parties is whether limitation [2] "a path configuring means," should be construed as a means-plus-function limitation under § 112, ¶ 6.[2] Judge Illston concluded that the limitation should be construed as a means-plus-function limitation governed by § 112, ¶ 6, and Intel urges that is the correct construction. The Court agrees with Judge Illston and Intel that this limitation should be construed as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6.

An initial question is the extent to which this Court is bound by Judge Illston's construction. Intel cites *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), arguing that the Court's comment relating to the "importance of uniformity in the treatment of a given patent,"

[1] Appendix A contains claim 1 of the patent with the currently disputed terms in bold.

[2] Judge Illston in her opinion added numbering to the claim limitations to facilitate discussion. The parties have continued to use those numbers in referring to specific limitations. Accordingly, claim 1 in Appendix A includes the numbering added by Judge Illston, shown in brackets.

favors "consistent claim construction for a given patent." Mitchell replies that collateral estoppel does not apply to Judge Illston's decision, citing *RF Delaware, Inc. v. Pacific Keystone Technologies, Inc.*, 326 F.3d 1255, 1261 (Fed. Cir. 2003)(discussing elements of collateral estoppel).

The Supreme Court's comment in *Markman* was in the context of explaining why claim construction was deemed a matter of law for the court, rather than an issue of fact for a jury. The Court wrote:

> Finally, we see the importance of uniformity in the treatment of a given patent as an independent reason to allocate all issues of construction to the court. It was just for the sake of such desirable uniformity that Congress created the Court of Appeals for the Federal Circuit as an exclusive appellate court for patent cases. Uniformity would, however, be ill served by submitting issues of document construction to juries.

Markman, 417 U.S. at 390-91. The Court added:

> But whereas issue preclusion could not be asserted against new and independent infringement defendants even within a given jurisdiction, treating interpretive issues as purely legal will promote (though it will not guarantee) intrajurisdictional certainty through the application of *stare decisis* on those questions not yet subject to interjurisdictional uniformity under the authority of the single appeals court.

Id. at 391.

Judge Illston's opinion was not appealed to the Federal Circuit, and Intel points to no authority that would accord that opinion issue preclusion or collateral estoppel effect. Nor does Intel assert that Mitchell is bound by principals of judicial estoppel. Indeed, the Federal Circuit recently held in *Lava Trading, Inc. v. Sonic Trading Management, LLC*., No. 05-1177, 2006 WL 1008842, at *3 (Fed. Cir. Apr. 19, 2006) that "judicial estoppel does not normally apply on appeal to prevent a party from altering an unsuccessful position before the trial court," and "estoppel would not bar Lava from departing from a claim construction theory unsuccessfully advocated before the trial court." *Id*; *see also SanDisk Corp. v. Memorex Prods., Inc.*, 415 F.3d 1278 (Fed. Cir.

2005)(generally disfavoring applying principals of estoppel to "evolving" claim construction).

Although not binding on this Court, Judge Illston's thoughtful and thorough opinion is nevertheless entitled to reasoned deference under the broad principals of *stare decisis* and the goals articulated by the Supreme Court in *Markman*, even though *stare decisis* may not be applicable *per se*. Accordingly, the Court accepts the premise that a uniform treatment of claim construction is desirable, but rejects Intel's suggestion that this Court is bound in any way to accept the claim construction by Judge Illston. This Court will take into account Judge Illston's claim construction as a thoughtful and thorough analysis of the parties' arguments involving the same patent and the same claim—but, in the end, will render its own independent claim construction. *See e.g., Exxon Chem. Patents, Inc. v. Lubrizol Corp.*, 64 F.3d 1553, 1555 (Fed. Cir. 1995)("The duty of the trial judge is to determine the meaning of the claims at issue, and to instruct the jury accordingly. In the exercise of that duty, the trial judge has an independent obligation to determine the meaning of the claims, notwithstanding the views asserted by the adversary parties.")(citations omitted). The Court does, however, agree with Judge Illston's opinion in most respects.

Mitchell argues that the disputed phrase should not be construed as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6 because claim 1, as a whole, recites sufficient structure and location for the "path configuring means" such that § 112, ¶ 6 does not apply. Mitchell asserts that the function of "path configuring" is to form paths. Mitchell argues that the memory address, data, and control circuits specified in limitations [6], [7], and [8] of claim 1 provide sufficient structure to perform that function. Mitchell further cites *Apex, Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003) for the proposition that the term "circuit" means "to form paths," arguing that the presence of the word "circuit" in element [6] of claim 1 is sufficient structure to perform the path configuring function. Mitchell additionally argues that [1] (the CPU limitation) and [3] (the control

circuit limitation) provide further structure to perform the path configuring function. Finally, Mitchell contends that limitations [9] and [10] of claim 1 indicate the location of the path configuring means. Mitchell also points to various sections of the specification arguing that the sections support its contention that limitations [1], [3], [6], [7], [8], [9], and [10] provide sufficient structure within claim 1 to perform the function of the path configuring means.

The use of the word "means" raises a presumption that § 112, ¶ 6 applies. *See Harris Corp. v. Ericsson Inc.*, 417 F.3d 1241, 1248 (Fed. Cir. 2005). This presumption can be overcome by a showing that the claim recites no function or provides sufficient structure, material, or acts to perform the recited function. *See Sage Prods., Inv. v. Devon Indus. Inc.*, 126 F.3d 1420, 1427 (Fed. Cir. 1997). The word "means" is sometimes used in instances where it is clear that "means" adds nothing to the limitation, *i.e.*, the limitation is structurally complete and the context of the claim suggests simply that the patent drafter was enamored with the word "means." *See e.g., Allen Eng'g Corp. v. Bartell Indus.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002); *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 531 (Fed. Cir. 1996). In general, the presumption imposes a burden on the party opposing the effect of the presumption to present evidence to rebut the presumption. In this case, the presence of the word "means" makes it Mitchell's burden to come forward with a showing rebutting the presumption. *See Apex*, 325 F.3d at 1372 (explaining that the burden flows from Rule 301 of the Federal Rules of Evidence). According to the Federal Circuit, "[t]his burden must be met by a preponderance of the evidence." *Id*. (citing *A.C. Aukerman Co. v. R.L. Chaides Constr. Co.*, 960 F.2d 1020, 1045 (Fed. Cir. 1992)). The Federal Circuit has explained that "[i]f the party who must bring forth evidence fails to proffer sufficient evidence to meet its burden, the presumption, either for or against the application of § 112, ¶ 6, prevails." *Id*.

Mitchell has not overcome the presumption that § 112, ¶ 6 applies. First, the word "means"

is used in connection with limitation [2] "a path configuring means," limitations [9] and [10], *i.e.*, "first" and "second" "switch means," and limitation [13] "means for causing . . . ." In the context of the claim as a whole, this suggests the drafter did not insert "means" indiscriminately or mechanically, such as in *Allen Engineering* and *Cole*, but rather chose when to use—and when not to use—the word "means." That "means" was intentional is further supported by the limitation. If "means" is deemed superfluous, the limitation would read "a path configuring," which on its face has no meaning. Grammatically, the "path configuring" phrase lacks an object. Here, the drafter chose to use the word "means" as the object, rather than a term or phrase that named or connoted structure, even in a generic sense.

Second, as Judge Illston observed: "Mitchell has not provided the Court with any other evidence, whether it be from a technical dictionary or any other reference, that a 'path configuring' device had a structure that was understood by people skilled in the art at the time of the invention." *Maurice Mitchell v. Samsung Elecs. Co., Ltd.*, slip op. at 8-9. In determining whether a claim term recites sufficient structure, courts examine whether it has an understood meaning in the art. *Watts v. XL Sys., Inc.*, 232 F.3d 877, 880-81 (Fed. Cir. 2000). To aid this determination, courts look at whether the "term, as the name for the structure, has a reasonably well understood meaning in the art," keeping in mind that a claim term "need not call to mind a single well-defined structure" to fall within the ambit of § 112, ¶ 6. *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996); *see also Lighting World, Inc. v. Birchwood Lighting, Inc.*, 382 F.3d 1354, 1359 (Fed. Cir. 2004). The record reveals no evidence that one of ordinary skill in the art would accord "path configuring" a structural connotation. Instead, the record reveals that this is a functional limitation.

In *Signtech USA Ltd. v. Vutek, Inc.*, 174 F.3d 1352, 1356 (Fed. Cir. 1999), the Federal Circuit observed that "[i]n this case, the claim element 'ink delivery means' uses the term 'means' in

association with a function, namely 'ink delivery.' Although the phrase 'means for' is not used, the phrase 'ink delivery means' is equivalent to the phrase 'means for ink delivery,' because 'ink delivery' is purely functional language." The claim language here is analogous. It is clear that "path configuring" states function, rather than structure, in a manner analogous to "ink delivery" in *Signtech*.

Mitchell's primary argument is that other limitations in the claim, principally limitations [6] through [8], provide the requisite structure for performing the claimed function. The Court disagrees; but, before turning to the substance of that argument, the Court must resolve the "function" recited in the term "a path configuring means."

Intel urges that limitations [6] through [8] (and/or other claim limitations) do not provide the structure necessary to perform the "path configuring" function as defined by Judge Illston. Mitchell disagrees that Judge Illston's discussion of the "function" of the "path configuring means" provides a basis for deciding whether limitations [6] through [8] (and/or other limitations in claim 1) recite structure sufficient to perform the claimed function.

A district court should not redefine the stated function in a means-plus-function limitation, *i.e.*, by expanding or narrowing the stated function. *See Micro Chem., Inc. v. Great Plains Chem. Co., Inc.* (*Micro Chem. II*), 194 F.3d 1250, 1258 (Fed. Cir. 1999)("The statute does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim. Nor does the statute permit incorporation of structure from the written description beyond that necessary to perform the claimed function.").

Judge Illston concluded that

> [t]he 'path configuring' function creates the path that dedicated memory address, data, and control signals follow at a particular time from among the variety of possible alternative signal paths within the path configuring means that permit the

> CPU to be interconnected with various alternative sets of contacts. 'Path configuring' involves creating one path in the path configuring means to permit the CPU to be interconnected to one set of contacts, and creating at a different time another path in the path configuring means to permit the CPU to be interconnected to another set of contacts.

Maurice Mitchell v. Samsung Elecs. Co., Ltd., slip op. at 10-11.

The parties' current disagreement as to whether Judge Illston accurately articulated the "function" intended by the claim language "path configuring" is largely due to Mitchell's wavering on the proper construction. In its opening brief, Mitchell urged that "path configuring means" should be construed as "the 'path configuring means' defined structurally by elements [1], [3], [6], [7] and [8] creates the path that dedicated memory address, data, and control signals follow at a particular time from among a variety of possible alternative signal paths within the path configuring means that permit the CPU to be interconnected with various alternative sets of contacts. 'Path configuring means' involves creating one path in the path configuring means to permit the CPU to be interconnected to one set of contacts, and creating at a different time another path in the path configuring means to permit the CPU to be interconnected to another set of contacts." Intel responded that both parties had accepted Judge Illston's construction of the "function" of the disputed phrase. Intel argued that the other limitations that Mitchell relied on in claim 1 could not perform those functions. In reply, Mitchell urged that "Plaintiff does not accept the path configuring function of Judge Illston since 'path configuring' means 'path forming.'"

In this instance, the Court must depart somewhat from Judge Illston's construction, recognizing that the parties here are advancing arguments and disagreements that may not have been highlighted before Judge Illston. Pursuant to *Micro Chemical II*, the stated function of the disputed phrase "a path configuring means" is "path configuring." The Court may not alter that stated function. Furthermore, that is the function that must be used to determine the "corresponding

structure" for performing that function, as well as whether limitations [6] through [8] recite sufficient structure for performing that function—not Judge Illston's construction of that function. *See Micro Chem. II*, 194 F.3d at 1258 (stating that "[a]n error in identification of the function can improperly alter the identification of structure in the specification corresponding to that function"). For the same reason, the Court rejects Mitchell's effort to "construe" the stated function as "path forming." Accordingly, the Court construes the function in claim 1 as "path configuring." That is the function that controls the analysis.

Turning then to Mitchell's argument that limitations [6] through [8] provide the structure for performing that function, the language and structure of the claims suggest otherwise. First, claim 1 begins by broadly calling for "[1] a Central Processing Unit (CPU)" and "[2] a path configuring means," as well as "[3] path control circuits connecting said CPU to said path configuring means." Contrary to Mitchell's suggestion that limitation [3] adds structure to the "path configuring means," that limitation clearly calls for "path control circuits" that connect the CPU "to said path configuring means." By the language of the claim, the "path control circuits" are not part of the "path configuring means."

Claim 1 then, using the phrase "wherein said CPU further comprises," additionally defines the CPU in limitation [5] as comprising "a dedicated memory address circuit." Similarly, limitation [6], using the same form of introductory phrase "wherein said path configuring means further comprises," additionally defines the "path configuring means" as comprising "a dedicated memory address circuit." Limitation [7] in the same fashion, "wherein each said dedicated memory address . . . circuit includes," then further defines those circuits. And limitation [8] further defines the memory control lines. In short, the structure and language of claim 1 first introduces the CPU and "path configuring means" as broad claim elements and then further defines or limits each of those

elements.

The terms "comprising," "comprises," and "includes" are open-ended terms. *See CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005)("'The transitional term "comprising" . . . is inclusive or open-ended and does not exclude additional, unrecited elements or method steps.' *Ga.-Pac. Corp. v. United States Gypsum Co.*, 195 F.3d 1322, 1327-28 (Fed. Cir. 1999). 'A drafter uses the term "comprising" to mean "I claim at least what follows and potentially more."' *Vehicular Techs. Corp. v. Titan Wheel Int'l, Inc.*, 212 F.3d 1377, 1383-84 (Fed. Cir. 2000)"); *Rocknel Fastener, Inc. v. United States*, 267 F.3d 1354, 1360 (Fed. Cir. 2001) ("That definition, which uses the term 'includes' and thus is open-ended, consists of three elements . . . .").

Thus, when the patentee began claim 1 with "[a] microcomputer . . . apparatus, comprising: . . . [2] a path configuring means," the claim at that juncture called for an undefined "means" for performing a "path configuring" function. Limitations [6] *et seq*., also open-ended ("further comprises"), further qualified or limited the "means," but did not exclude further components. Indeed, that is clear from the claims that follow claim 1.

For example, claim 2 adds that the "path configuring means" of claim 1 "further includes" a "first internal buss [*sic*.]." *See* Col. 91:38-56. And claim 3 adds that the "path configuring means" of claim 1, as further defined in claim 2, "is further comprised of" "third," "fourth" and "fifth" "switch means" *etc*. *See* Cols. 91:57-92:2.

Thus, the claim language itself suggests that whatever structure is recited in limitations [6] through [8] in claim 1 alone may not be necessarily sufficient to perform the stated "path configuring" function. That is, limitations [6] through [8] in claim 1 may add structure in the form of dedicated memory address, data and control circuits, but doing so does not necessarily provide sufficient structure to perform the function of "path configuring" without, for example, the several

"switch means" of claim 3.

The Court also rejects Mitchell's contention that the word "circuit" in element [6] of claim 1 provides sufficient structure to perform the "path configuring" function. First, *Apex* is distinguishable from the present case because in *Apex*, the word "circuit" was found to connote some structure but in the absence of the word "means" and without the presumption that § 112, ¶ 6 applied. *See* 325 F.3d at 1373. Here, there is a presumption that § 112, ¶ 6 applies, and the word "circuit" is not found in the disputed term. Moreover, the specification indicates that the "switching unit," described in Figure 1, is the structure that performs the function of configuring paths:

> The memory access circuits (address, data, control) of the CPU are connected to a switching unit. Three buses, "A", "B"and "C" are connected to the switching unit. The internal structure of the switching unit is configured solely by the CPU to create a signal path connecting the memory access circuits of the CPU to the desired bus or buses or any selected portion thereof.

Col. 7:37-44. Furthermore, even if "circuit" was deemed structural, the fact remains that the actual recited structure of elements [6] through [8] is insufficient to perform the "path configuring" function for the reasons discussed above.

Accordingly, the Court agrees with Judge Illston that this "limitation clearly states a function for the means, namely 'path configuring.'" *Maurice Mitchell v. Samsung Elecs. Co., Ltd.*, slip op. at 9. Although Judge Illston went on to adopt a "construction" of the "path configuring" function, and although that construction appears to be accurate in terms of the specification, the Court, as noted above, is bound by the actual stated function in the claim. Further, in light of the foregoing, that additional construction is not necessary to resolve the parties' dispute.

The Court agrees with Judge Illston and Intel and identifies the corresponding structure as "the structure described in the specification for performing the path configuring function is a structure having the first through fifth internal buses, the junction, and the third through seventh

switch means arranged as shown in Switching Unit 100 of Figure 1 and described in the specification. The dedicated memory, address, data, and control circuits of the path configuring means as required in the sixth limitation, are the circuits that make up those internal buses, junction, and switch means. As required in the seventh limitation, each such dedicated memory address, data, and control circuit includes a plurality of dedicated memory address, data, and control lines." Mitchell does not provide a proposed corresponding structure for the "path configuring means." However, Intel's proposed structure is identical to the structure identified by Judge Illston in her Claim Construction Order.

Judge Illston, noting that there was "some discussion" of the structure at several points in the specification, went on to describe that structure. In doing so, Judge Illston used language that appears in the specification, and in other claims, for example claims 2 and 3, but not claim 1. Furthermore, Judge Illston refers to "the first through fifth internal buses" and the "third through seventh switch means." Those terms do not appear in claim 1. However, as noted above, other claims, for example claims 2 and 3, provide that the "path configuring means" of claim 1 is "further comprised" of those elements. Accordingly, the Court agrees with Judge Illston and Intel that the corresponding structure is "the structure described in the specification for performing the path configuring function is a structure having the first through fifth internal buses, the junction, and the third through seventh switch means arranged as shown in Switching Unit 100 of Figure 1 and described in the specification."

The Court further agrees with Judge Illston that limitation [6] in claim 1 includes the dedicated memory, address, data, and control circuits, as further defined in limitations [7] through [8], as part of the path configuring means. The Court also agrees with Judge Illston that limitation [7] in claim 1 provides that "each said dedicated memory address, data, and control circuit includes

a plurality of dedicated memory address, data, and control lines respectively," and thus the corresponding structure includes such lines. Finally, although they are not required by limitation [6] of claim 1, it is clear that buses, junctions and switch means 3 through 7 are added by claims 2 and 3 and constitute part of the "path configuring means."

For the reasons expressed above, the Court identifies the structure of the "path configuring means" consistently with Judge Illston's previous Claim Construction Order.

"path control circuits connecting said CPU to said path configuring means"

The Court and the parties agree that the term should be construed as "circuits that physically connect the CPU to the path configuring means, and that operate on input signals from the CPU and generate appropriate output signals to control the path configuring means, and thereby create the path for memory address, data and control signals to follow along various alternative possible paths."

"a plurality of contacts comprised of a plurality of distinct sets"

The Court and the parties agree that the term should be construed as "a plurality of physically distinguishable sets (that is, collections) of electrical contacts with each set (or collection) having contacts for memory address, data, and control signals. A 'contact' is a conductor, such as a pad of metal on a semiconductor chip or a pin, for physically connecting with another such conductor to permit current to flow between the two conductors."

"wherein said CPU further comprises a dedicated memory address circuit, a dedicated memory data circuit, a dedicated memory control circuit and a dedicated power circuit"

The Court and the parties agree that the term should be construed as "the CPU contains four circuits. A 'circuit' means an arrangement of electronic components interconnected by lines that has at least one input and one output terminal, and whose purpose is to produce at the output

terminal a signal that is a function of the signal at the input terminal. A 'circuit' is not a line. A 'dedicated' circuit means a circuit that provides a clear unbroken communications path from one station to another and that is always available for use. A 'dedicated memory' circuit means a circuit that is always available for the purpose of transmitting signals between the CPU and memory. 'Memory' means the addressable storage in which instructions and other data are stored and retrieved for execution and processing. A 'dedicated power circuit' means a circuit that is always available to provide power to the CPU. One of the four circuits is a 'dedicated memory address circuit' meaning a circuit that is always available to transmit signals representing memory addresses between the CPU and memory. Another is 'a dedicated memory data circuit' meaning a circuit that is always available to transmit signals representing data for storage in memory between the CPU and memory. Another is 'dedicated memory control circuit,' meaning a circuit that is always available to carry signals representing memory control functions between the CPU and memory."

"wherein said path configuring means further comprises a dedicated memory address circuit, a dedicated memory data circuit and a dedicated memory control circuit"

The Court and the parties agree that the term should be construed as "the path configuring means contains three types of circuits. One is a 'dedicated memory address circuit,' meaning a circuit that is always available to transmit signals representing memory addresses to memory. Another is 'a dedicated memory data circuit,' meaning a circuit that is always available to transmit signals representing data to or from memory. Another is 'a dedicated memory control circuit,' meaning a circuit that is always available to transmit signals representing memory control functions to or from memory."

"wherein each said dedicated memory address, data and control circuit includes a plurality of dedicated memory address, data, and control lines respectively"

The Court and the parties agree that the term should be construed as "each dedicated memory

address circuit of the CPU and the path configuring means has a plurality of dedicated memory address lines. Each dedicated memory data circuit of the CPU and the path configuring means has a plurality of dedicated memory data lines. Each dedicated memory control circuit of the CPU and the path configuring means has a plurality of dedicated memory control lines. A 'line' is a conductor that may be used to carry a signal."

"wherein said memory control lines are comprised of a read /- write line, timing lines and status lines"

The Court and the parties agree that the term should be construed as "the dedicated memory control lines of the CPU and path configuring means include a single line that carries read and write signals, a plurality of memory lines that carry timing signals, and a plurality of memory lines that carry status signals."

"first switch means comprised of at least three distinct parts for connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts"

The Court agrees with Intel that this limitation should be construed as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6. Mitchell argues that the "first switch means" is not a means-plus-function limitation. Mitchell contends that "switch" is a structural term and argues that claim 1 recites sufficient structure and location to perform the function of the "first switch means."

Mitchell cites *Vitronics*, 90 F.3d at 1584, for the proposition that the term "switch" is commonly used and understood as a structural element by those skilled in the art. Mitchell also points to the IEEE Dictionary, which provides multiple definitions of the word "switch," one being "a device for making, breaking or changing the connections in an electrical circuit." Mitchell contends that the use of the word "means" in association with the word "switch" does not necessitate the application of § 112, ¶ 6. Mitchell also cites two district court opinions where courts found that

"switch means" was not subject to § 112, ¶ 6 because the claim language recited sufficient structure and or location to rebut the presumption of its application. *See Gen. Creation v. Leapfrog Enters., Inc.,* 232 F. Supp. 2d 661, 672-73 (W.D. Va. 2002); *MediaCom Corp. v. Rates Tech., Inc.*, 4 F. Supp. 2d 17, 27 (D. Mass. 1998).

Mitchell further argues that the specification supports its contention that the "switch means" is not subject to § 112, ¶ 6. Mitchell cites column 19, lines 38 through 41, which state, "These switches are utilized to connect the address, data and control lines necessary for the proper memory access between the buses," and column 19, line 64 through column 20, line 5, which state that each first through seventh switch means "actually represents a plurality of logical elements, each of which can logically connect or logically disconnect an address, data, or control circuit that is mechanically connected to the switch means . . . ." Finally, Mitchell contends that claim language itself identifies the location of the structure as between the dedicated memory address, data, and control circuits of the path configuring means and the sets of contacts.

Intel argues that the presumption that § 112, ¶ 6 applies has not been overcome because the claim does not identify sufficient structure to perform all of the recited functions of the switch means. The parties do not dispute that the stated function of the "first switch means" is "for connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts." Also, the claim provides that the "first switch means" is "comprised of three distinct parts." Therefore, as with "path configuring means," the question becomes whether the claim recites sufficient structure, material, or acts to perform the recited function."

In the context of the '154 patent, the word "switch" itself does not connote sufficient structure to overcome the presumption that § 112, ¶ 6 applies. Unlike the district court cases cited

by Mitchell, in *Overhead Door Corp. v. Chamberlin Group, Inc.*, the Federal Circuit held that "second switch means" was subject to § 112, ¶ 6 because "this claim element utilizes the term 'means' and the claim does not specify any structure or material for performing the recited function." 194 F.3d 1261, 1271 (Fed. Cir. 1999). The Federal Circuit did not find that the word "switch" provided sufficient structure to overcome the presumption that § 112, ¶ 6 applied.

Contrary to Mitchell's argument, in deciding whether a particular limitation should be construed as a means-plus-function limitation or not, the issue is not solely whether a dictionary definition can be found for a term, but rather how a claim limitation should be construed in the manner intended by the drafter. Insofar as § 112, ¶ 6 is concerned, an applicant has a choice whether to invoke both the advantages and disadvantages of presenting means-plus-function limitations—or not. An applicant signals an intent to invoke the advantages and disadvantages of § 112, ¶ 6 by using the word "means." Similarly, an applicant signals an intent not to invoke the advantages and disadvantages of § 112, ¶ 6 by not using the word "means." Although the presence or absence of the word "means" is not necessarily dispositive, the Federal Circuit, drawing on the foregoing rationale, has explained that the presence or absence of the word "means" creates a rebuttable presumption that § 112, ¶ 6 applies, or does not apply, respectively. The Federal Circuit has stressed that "[t]he use of the term 'means' is 'central to the analysis,' . . . because the term 'means,' particularly as used in the phrase 'means for,' is 'part of the classic template for functional claim elements,' . . . and has come to be closely associated with means-plus-function claiming." *Lighting World*, 382 F.3d at 1358. Accordingly, the Federal Circuit has labeled that presumption "a strong one that is not readily overcome." *Id*.

Here, the patentee has signaled that he intended to invoke § 112, ¶ 6 by using the word "means." As noted above, there are cases in which it is clear that "means" added nothing to a claim,

and that the patent drafter was simply enamored with the word "means." *See e.g., Allen Eng'g*, 299 F.3d at 1348; *Cole*, 102 F.3d at 531. As also noted above, here the patentee chose to use the word "means" in connection with limitation [2] "a path configuring means," limitations [9] and [10], *i.e.*, "first" and "second" "switch means," and limitation [13] "means for causing . . . ." Thus, unlike cases such as *Allen Engineering* and *Cole*, the intrinsic record suggests that the drafter here chose selectively when to use—and when not to use—the word "means."

Thus, during prosecution, the patentee signaled his intention to invoke § 112, ¶ 6 by using the word "means," and in doing so created the aforementioned "strong" presumption. Although that presumption is certainly rebuttable, Mitchell has presented no persuasive reason why the patentee should not be held to that choice, especially given that "switch" has both structural and functional connotations and that the patentee most frequently used "switch" in a functional context.

Mitchell, relying on an IEEE Dictionary definition of "switch," urges that "switch" is defined as "a device for making, breaking or changing the connections in an electrical circuit." But Mitchell does not rely on that definition in urging its proposed claim construction. Rather, Mitchell urges that the "first switch means" and "second switch means" limitations should be construed as:

> The first switch means is a mechanism including one first part for connecting those circuits at one end of one path of the path configuring means to one distinct set of contacts and to disconnect those circuits from that one set of contacts. A second part of the mechanism acts by switching to connect those circuits at the end of a second path of the path configuring means to a second distinct set of contacts and to disconnect those circuits from that set. A third part of the mechanism acts by switching to connect those circuits at the end of a third such path of the path configuring means to a third distinct set of contacts and to disconnect those circuits from those contacts. Each part of the switch means connects and disconnects the memory address, data and control circuits of the path configuring means to or from one of the distinct sets of contacts.
>
> The second switch means is a mechanism to connect the dedicated memory address, data, and control lines of the path configuring means to the dedicated memory address, data, and control lines of the CPU respectively, and to disconnect those lines from each other.

Thus, Mitchell proposes an expansive, functional construction having little to do with the proffered definition of "switch."

Claim construction is to resolve the disputed meaning of a term or phrase—not an invitation for wholesale claim revision. Although it is recognized that Mitchell's functional description is patterned after Judge Illston's explanation of the function served by the "first" and "second" "switch means," the actual limitations of claim 1 simply provide:

> [9] first switch means comprised of at least three distinct parts for connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts, and
>
> [10] second switch means for connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively.

That is, if Mitchell's argument that § 112, ¶ 6 should not apply was accepted, elements [9] and [10] would simply be viewed without the word "means."

Second, Mitchell does not address the situation where a term can have both structural and functional connotations and seems to assume that if a term has a structural connotation the presumption should be deemed rebutted because using "means" results in a narrower construction than if "means" is not used. That is not necessarily the case.

In *Overhead Door*, for example, although the term "switch" had a structural connotation, the Federal Circuit recognized that "switch" also has a functional connotation that potentially prevails when used with "means." *See* 194 F.3d at 1271. Moreover, *Overhead Door* illustrates that although "switch" may have a structural connotation as a noun, "switch" likewise has a functional connotation, and the structural connotation does not trump the patentee's choice to invoke § 112, ¶ 6 by using "switch means," at least where there is no evidence in the intrinsic record to the contrary. Mitchell has pointed to no such evidence.

Third, the Federal Circuit has looked to the specification to determine whether a term has

been used to define structure. *See Lighting World*, 382 F.3d at 1361 ("it is clear that the parties in this case have used that term to denote structure. The written description of the [patent-in-suit], for example, uses the term 'connector assembly' as the name for structure."). Here, throughout the specification of the '154 patent, the most frequently used term is "switch means," rather than simply "switch." *See* Col. 19:53-60. The specification also explains that a "switch means" is a "switching device" under the control of the microcomputer. For example, the specification explains that "[t]he fifth switch means 112 is a switching device, under the control of the BICPU microcomputer, that can logically connect and logically disconnect the circuit between the common junction point and the 'B' bus circuits 128 . . . ," Col. 20:44-49; "[t]he sixth switch means 114 is a switching device, under the control of the BICPU microcomputer, that can logically connect and logically disconnect the circuit between common junction point and the 'C' bus circuits 132 . . . ," Col. 21:31-38. The specification thus indicates that the patentee did not use "switch" in "switch means" in a structural sense, but rather in a functional sense (*i.e.*, a "means" for providing a "switch" function), and used another term, for example "switching device," to refer to structure.

The patentee chose to use the word "means" thus signaling an intent to invoke § 112, ¶ 6. That raises the presumption that § 112, ¶ 6 applies. The term "switch" has both structural and functional connotations. If the patentee had wished to rely on the structural connotation, the patentee could have used "a switch," or a "switching device," or even a generic structural term, but did not. Rather, the patentee used "switch means," as he did throughout the specification, in a context indicating that "switch" was being used functionally, not structurally. Overall, Mitchell has not provided persuasive evidence that the presumption arising from using the term "means" has been rebutted. *Compare Interspiro USA Inc. v. Figgie Int'l Inc.*, 815 F. Supp. 1488, 1504 (D. Del. 1993), *aff'd*, 18 F.3d 927,930-31 (Fed. Cir. 1994)(agreeing with the district court's construction of "detent

means . . . for . . . " as a means-plus-function limitation), *with Greenberg*, 91 F.3d at 1584 (construing "detent mechanism" as defining structure, reasoning "[w]hile the language in the *Interspiro* case was in classic 'means-plus-function' format, the language in Dr. Greenberg's patent was not.").

Having concluded that the "first switch means" is a means-plus-function limitation governed by § 112, ¶ 6, the Court construes the function of the "first switch means" as "connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts." *See Micro Chem. II*, 194 F.3d at 1258.

Judge Illston "construed" the function of the "first switch means" apparently due to a disagreement of the parties in which Mitchell was proposing a construction that did not differentiate between the "first" and "second" "switch means." *Maurice Mitchell v. Samsung Elecs. Co., Ltd.*, slip op. at 19-20. Intel has now proposed a construction of the "function" of the "first switch means" that is identical to Judge Illston's construction, but with an addition that Mitchell opposes. Mitchell, while contending that "first switch means" should not be construed under § 112, ¶ 6, has nevertheless proposed a construction that also substantively tracks Judge Illston's construction with minor changes, for example using "mechanism" rather than "means." To the extent that there was any previous disagreement as to the "three distinct parts," that disagreement no longer exists. Both Mitchell's and Intel's proposed constructions use the identical language.

Claim construction is intended to resolve disputes between the parties on the meaning of claim terms and phrases. *See Vivid Techs., Inc. v. Am Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those [claim] terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy."). Because there is no longer any dispute between the parties there is no need for the Court to "construe" the "function" of limitation [9]. For the same

reason, the Court rejects Intel's proffered addition to Judge Illston's construction.

Intel urges that the specification discloses no corresponding structure for performing the stated function. Judge Illston held the same. Mitchell, on the other hand, points to several places in the specification as allegedly disclosing such structure.

Intel suggests that this issue should be deferred to summary judgment. The Court agrees. The Federal Circuit has held that whether sufficient structure is disclosed in a specification must be based on the understanding of one skilled in the art, and asserting that a means-plus-function limitation lacks structural support requires clear and convincing evidence because the consequence is invalidity. *See Creo Prods, Inc. v. Presstek, Inc.*, 305 F.3d 1337, 1347 (Fed. Cir. 2002); *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376-80 (Fed. Cir. 2001); *S3 Inc. v. nVIDIA Corp.*, 259 F.3d 1364, 1371 (Fed. Cir. 2001); *Atmel Corp. v. Info. Storage Devices, Inc.*, 198 F.3d 1374, 1382 (Fed. Cir. 1999). The Federal Circuit has further held that "corresponding structure" does not require a disclosure of specific circuitry. *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1366-67 (Fed. Cir. 2003).

Accordingly, the issue of whether there is (or is not) "corresponding structure" disclosed in the specification for performing the claimed functions, and if so what that structure may be, is deferred to summary judgment proceedings.

"second switch means for connecting said dedicated memory address, data , and control lines of said path configuring means to said dedicated memory address, data and control lines of said CPU respectively"

The Court agrees with Intel that this limitation should be construed as a means-plus-function limitation under 35 U.S.C.§ 112, ¶ 6. As with the "first switch means," Mitchell argues that "second switch means" should not be construed as a means-plus-function limitation under § 112, ¶ 6. Mitchell provides essentially the same arguments as it did in reference to "first switch means,"

except that here, Mitchell argues that the claim language identifies the location of the "second switch means" between the dedicated memory address, data, and control lines of the path configuring means and the dedicated memory address, data and control lines of the CPU. However, for the same reasons discussed above with regard to "first switch means," "second switch means" is construed as a means-plus-function limitation under § 112, ¶ 6.

Similarly, also for the same reasons discussed above, the Court declines to adopt the parties' proposed "constructions" of the stated function, as well as Intel's proposed additional language. The stated function of the "second switch means" is "connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data and control lines of said CPU respectively."

Also for the reasons discussed above, the issue of whether there is (or is not) "corresponding structure" disclosed in the specification for performing the claimed function, and if so, what that structure is, is deferred to summary judgment proceedings.

"*wherein said first and second switch means assume a non signal-conducting state when said CPU power circuit is not supplied with power*"

The Court agrees with Mitchell and construes the term as, "the eleventh limitation describes a further function performed by the first and second switch means. When the CPU power circuit is not supplied with power, the switch means takes on a state in which no current or voltage may be conducted through the switch, and therefore a voltage representing a signal on a line connected to one side of the switch will not be affected by and will not affect a voltage representing a signal on a line connected to the other side of the switch. This also means that a voltage representing a signal on a line connected to the switch will not be transmitted through the switch." Intel's proposed construction is almost identical to Mitchell's except that Intel argues that the words "when" and

"assume" should be construed and proposes additional language to construe the two words: "the 'assumption' of a non signal-conducting state occurs in response to, and continues as long as, the CPU power circuit is not supplied with power." Intel argues that the additional language will help the jury understand that "the claim requires the assumption of the non signal-conducting state to be a response to . . . the moment when the CPU gains power and sends an 'appropriate' signal to the 'switch means.'" Intel argues that "the purpose of the eleventh limitation is to isolate the elements of the system from each other in the event the CPU is damaged and to remain in that isolated state until receipt of an appropriate signal from the CPU." *See* Col. 3:5-13; Col. 42:47-53; Cols. 43:65-44:20.

The additional language proposed by Intel is not supported by the claim language and is not necessary. Furthermore, this additional language was not included in Judge Illston's construction. Accordingly, Intel's proposed addition language is not included in the Court's construction of the limitation.

"*wherein said lines of said CPU and said contacts assume a non signal-conducting state when said first and second switch means are in said non signal-conducting state*"

The Court agrees with Mitchell and construes the term as, "the dedicated memory address data, and control lines of the CPU and the dedicated memory address, data and control lines of each of the three sets of contacts assume a non signal-conducting state when the first and second switch means are in a non signal-conducting state. Accordingly, those lines take on a state in which no current or voltage may be conducted through them, and voltages representing signals on the lines may not be transmitted along the lines, whenever the first and second switch means are also in this state." Again, Intel's proposed construction is nearly identical to Mitchell's except that Intel argues that the words "assume" and "when" should be construed and proposes additional language that

states, "the 'assumption' of a non signal-conducting state by the lines and contacts occur in response to, and continues as long as, the first and second 'switch means' are in a non signal-conducting state," to accomplish this goal.

For the same reasons discussed above with regard to the eleventh limitation, Intel's additional language is rejected and the Court construes the term consistently with Judge Illston's construction.

"means for causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU and to"

and

"*assume a non signal-conducting state upon receipt of an appropriate signal from said CPU*

The Court and the parties agree that these limitations should be construed as means-plus-function limitations under 35 U.S.C.§ 112, ¶ 6.

Intel and Mitchell have proposed "constructions" of the stated functions that are substantively identical, except that Intel has proposed additional language. The "constructions" that the parties propose—like the proposed constructions in connection with the "first" and "second" "switch means" limitations above—go far beyond the actual language of the claim. As discussed above, in identifying the stated function, the Court is constrained to the actual language of the claim. Also, there does not appear to be any dispute between the parties as to the meaning of the claim language—except, again, that Intel proposes adding an additional two sentences, which Mitchell opposes.

Accordingly, the Court concludes that the stated functions are: (1) "causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal-conductive state upon receipt of an appropriate signal

from said CPU," and (2) "assume a non signal-conducting state upon receipt of an appropriate signal from said CPU."

The Court agrees with Intel and identifies the corresponding structure as, "to the extent that any structure for the corresponding function of the thirteenth and fourteenth limitations is provided in the specification, that structure is described at col. 24:67 – col. 25:56." Mitchell agrees that the limitation should be construed as a means-plus-function limitation under § 112, ¶ 6 but does not provide a proposed structure in its Opening Brief or in the Joint Claim Construction Chart. Mitchell appears to object to Intel's proposed structure in its Opening Brief but offers no support for its objection. Intel's proposed structure is identical to the structure identified by Judge Illston in her Claim Construction Order. Accordingly, and because Mitchell fails to provide an alternative structure, the Court identifies the corresponding structure consistent with Judge Illston's Claim Construction Order.

CONCLUSION

For the foregoing reasons, the Court interprets the claim language in this case in the manner set forth above. For ease of reference, the Court's claim interpretations are set forth in a table as Appendix B. The claims with the disputed terms in bold are set forth in Appendix A.

So ORDERED and SIGNED this 21st day of June, 2006.

LEONARD DAVIS
UNITED STATES DISTRICT JUDGE

APPENDIX A

1. A microcomputer data processing apparatus, comprising:

[1] a Central Processing Unit (CPU),

[2] a **path configuring means**,

[3] path control circuits connecting said CPU to said path configuring means,

[4] a plurality of contacts comprised of a plurality of distinct sets,

[5] wherein said CPU further comprises a dedicated memory address circuit, a dedicated memory data circuit, a dedicated memory control circuit and a dedicated power circuit,

[6] wherein said path configuring means further comprises a dedicated memory address circuit, a dedicated memory data circuit and a dedicated memory control circuit,

[7] wherein each said dedicated memory address, data, and control circuit includes a plurality of dedicated memory address, data, and control lines respectively,

[8] wherein said memory control lines are comprised of a read/write line, timing lines and status lines,

[9] **first switch means comprised of at least three distinct parts for connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts**, and

[10] **second switch means for connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively**.

[11] **wherein said first and second switch means assume a non signal-conducting state when said CPU power circuit is not supplied with power,**

[12] **wherein said lines of said CPU and said contacts assume a non-signal conducting state when said first and second switch means are in said non-signal conducting state,**

[13] **means for causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal-conductive state upon receipt of an appropriate signal from said CPU, and to**

[14] **assume a non signal-conducting state upon receipt of an appropriate signal from said CPU**.

APPENDIX B

CLAIM CONSTRUCTION FOR U.S. PATENT NO. 4,875,154

Claim Language	Court's Construction
a microcomputer data processing apparatus, comprising:	A single microcomputer, which includes, at the least, a microprocessor, storage (*e.g.* memory) and input/output device enabling the system to perform operations on data, which comprises what is set forth in the claim.
a Central Processing Unit (CPU)	The unit of a computing system having the circuits that control the interpretation of instructions and their execution. A CPU includes, at least, an arithmetic logic unit and associated registers.
a path configuring means,	**Function**: Path configuring **Structure**: The structure described in the specification for performing the path configuring function is a structure having the first through fifth internal buses, the junction, and the third through seventh switch means arranged as shown in Switching Unit 100 of Figure 1 and described in the specification. The dedicated memory, address, data, and control circuits of the path configuring means as required in the sixth limitation, are the circuits that make up those internal buses, junction, and switch means. As required in the seventh limitation, each such dedicated memory address, data, and control circuit includes a plurality of dedicated memory address, data, and control lines.
path control circuits connecting said CPU to said path configuring means	Circuits that physically connect the CPU to the path configuring means, and that operate on input signals from the CPU and generate appropriate output signals to control the path configuring means, and thereby create the path for memory address, data and control signals to follow along various alternative possible paths.
a plurality of contacts comprised of a plurality of distinct sets	A plurality of physically distinguishable sets (that is, collections) of electrical contacts with each set (or collection) having contacts for memory address, data, and control signals. A "contact" is a conductor, such as a pad of metal on a semiconductor chip or a pin, for physically connecting with another such conductor to permit current to flow between the two conductors.
wherein said CPU further comprises a dedicated memory address circuit, a dedicated memory data circuit, a dedicated memory control circuit and a	The CPU contains four circuits. A "circuit" means an arrangement of electronic components interconnected by lines that has at least one input and one output terminal, and whose purpose is to produce at the output terminal a signal that is a function of the signal at the input terminal. A "circuit" is not a line. A "dedicated" circuit means a circuit that provides a clear

dedicated power circuit	unbroken communications path from one station to another and that is always available for use. A "dedicated memory" circuit means a circuit that is always available for the purpose of transmitting signals between the CPU and memory. "Memory" means the addressable storage in which instructions and other data are stored and retrieved for execution and processing. A "dedicated power circuit" means a circuit that is always available to provide power to the CPU. One of the four circuits is a "dedicated memory address circuit" meaning a circuit that is always available to transmit signals representing memory addresses between the CPU and memory. Another is "a dedicated memory data circuit" meaning a circuit that is always available to transmit signals representing data for storage in memory between the CPU and memory. Another is "a dedicated memory control circuit," meaning a circuit that is always available to carry signals representing memory control functions between the CPU and memory.
wherein said path configuring means further comprises a dedicated memory address circuit, a dedicated memory data circuit and a dedicated memory control circuit	The path configuring means contains three types of circuits. One is a "dedicated memory address circuit," meaning a circuit that is always available to transmit signals representing memory addresses to memory. Another is "a dedicated memory data circuit," meaning a circuit that is always available to transmit signals representing data to or from memory. Another is "a dedicated memory control circuit," meaning a circuit that is always available to transmit signals representing memory control functions to or from memory.
wherein each said dedicated memory address, data and control circuit includes a plurality of dedicated memory address, data, and control lines respectively	Each dedicated memory address circuit of the CPU and the path configuring means has a plurality of dedicated memory address lines. Each dedicated memory data circuit of the CPU and the path configuring means has a plurality of dedicated memory data lines. Each dedicated memory control circuit of the CPU and the path configuring means has a plurality of dedicated memory control lines. A "line" is a conductor that may be used to carry a signal.
wherein said memory control lines are comprised of a read /- write line, timing lines and status lines	The dedicated memory control lines of the CPU and path configuring means include a single line that carries read and write signals, a plurality of memory lines that carry timing signals, and a plurality of memory lines that carry status signals.
first switch means comprised of at least three distinct parts for connecting said dedicated memory address, data, and control circuits of said path configuring means to each	**Function**: For connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts **Structure**: Deferred to summary judgment proceedings

of said first three sets of contacts	
second switch means for connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively	**Function**: For connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively. **Structure**: Deferred to summary judgment proceedings
wherein said first and second switch means assume a non signal-conducting state when said CPU power circuit is not supplied with power	The eleventh limitation describes a further function performed by the first and second switch means. When the CPU power circuit is not supplied with power, the switch means takes on a state in which no current or voltage may be conducted through the switch, and therefore a voltage representing a signal on a line connected to one side of the switch will not be affected by and will not affect a voltage representing a signal on a line connected to the other side of the switch. This also means that a voltage representing a signal on a line connected to the switch will not be transmitted through the switch.
wherein said lines of said CPU and said contacts assume a non signal-conducting state when said first and second switch means are in said non signal-conducting state	The dedicated memory address data, and control lines of the CPU and the dedicated memory address, data and control lines of each of the three sets of contacts assume a non signal-conducting state when the first and second switch means are in a non signal-conducting state. Accordingly, those lines take on a state in which no current or voltage may be conducted through them, and voltages representing signals on the lines may not be transmitted along the lines, whenever the first and second switch means are also in this state.
means for causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU and to and assume a non signal-conducting state upon receipt of an appropriate signal from said CPU.	**Function**: (1) Causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU. (2) Assume a non-signal conducting state upon receipt of an appropriate signal from said CPU. **Structure**: To the extent that any structure for the corresponding function of the thirteenth and fourteenth limitations is provided in the specification, that structure is described at col. 24:67 - col. 25:56.